Amendments to the Claims:

Without prejudice, this listing of the claims replaces all prior versions and listings of the claims in the present application:

Listing of Claims:

1.-8. (Canceled)

9. (Currently Amended) A method of manufacturing semiconductor components, the method comprising:

introducing depressions into a wafer of a first conductivity type;

coating both sides of the wafer with doping atoms;

carrying out a diffusion process;

dicing the wafer into individual chips in such a way that each chip includes at least one of the depressions in an internal area thereof but not in any edge area thereof; ~~and~~

sawing the depressions; and

applying metal layers to a first layer and a third layer of the wafer.

10. (Previously Presented) The method according to claim 9, wherein the depressions are formed as pits having a rectangular cross section.

11. (Previously Presented) The method according to claim 9, further comprising applying metal layers to both sides of the wafer before the wafer is diced.

12. (Previously Presented) The method according to claim 9, wherein the wafer is diced in areas of the wafer where no depressions have been introduced.

13. (Previously Presented) The method according to claim 9, further comprising covering a top side of the wafer using a dopant of a second conductivity type.

14. (Previously Presented) The method according to claim 9, further comprising covering a bottom side of the wafer using a dopant of the first conductivity type.

15. (Canceled)

16. (Currently Amended) A semiconductor component comprising:

a first layer of a first conductivity type having a top side and a bottom side, the first layer having areas of different thickness due to at least one depression introduced into the top side;

a second layer of a second conductivity type covering the top side of the first layer; and

a third layer situated on the bottom side of the first layer,

wherein the first layer, the second layer, and the third layer are diced into individual chips so that, in an internal area, each of the chips has at least one depression, ~~and~~

wherein the depression in an internal area is sawed and none of the first layer, the second layer, and the third layer include edge areas that have depressions;

wherein metal layers are applied to the first layer and the third layer.